

**INSTALLATION AND OPERATION** 

# **USER MANUAL**

WWW.UNICORECOMM.COM

# **UM960L**

GPS/BDS/GLONASS/Galileo/QZSS
All-constellation Multi-frequency
High Precision RTK Positioning Module

# **Revision History**

Version	Revision History	Date
R1.0	First release	Aug., 2022
	Update Pin14 description	
	Update section 2.1 Dimensions	
	Add section 3.1 Recommended Minimal Design	
R1.1	Optimize section 3.2 Antenna Feed Design	Mar., 2022
	Optimize section 3.3 Power-on and Power-off	
	Add section 3.5 Recommended PCB Package Design	
	Update the working current;	

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# **Foreword**

This document describes the information of the hardware, package, specification and the use of Unicore UM960L modules.

# **Target Readers**

This document applies to technicians who possess the expertise on GNSS receivers.



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### 1 Introduction

UM960L is a new generation of GNSS high precision positioning RTK module from Unicore. It supports all constellations and multiple frequencies, and can simultaneously track GPS L1/L2/L5 + BDS B1I/B2I/B3I + GLONASS G1/G2 + Galileo E1/E5a/E5b + QZSS L1/L2/L5. The module is mainly used in geological hazard monitoring, deformation monitoring, and high precision GIS.

UM960L is based on NebulasIV<sup>™</sup>, a GNSS SoC which integrates RF-baseband and high precision algorithms. Besides, the SoC integrates a dual-core CPU, a high speed floating point processor and a RTK co-processor with 22 nm low power design, and it supports 1408 super channels. All these above enable stronger signal processing.

UM960L features a compact size of 16.0 mm × 12.2 mm. It adopts SMT pads, supports standard pick-and-place, and supports fully automated integration of reflow soldering.

Furthermore, UM960L supports interfaces such as UART, I<sup>2</sup>C\*, which meets the customers' needs in different applications.

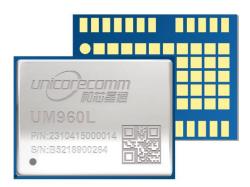


Figure 1-1 UM960L Module

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<sup>\*</sup> Reserved interface, not supported currently.



### 1.1 Key Features

- High precision, compact size and low power consumption
- Based on the new generation GNSS SoC -NebulasIV<sup>™</sup>, with RF-baseband and high precision algorithms integrated
- 16.0 mm × 12.2 mm × 2.4 mm, surface-mount device
- Supports all-constellation multi-frequency on-chip RTK positioning solution
- Supports GPS L1/L2/L5 + BDS B1I/B2I/B3I + GLONASS G1/G2 + Galileo E1/E5b/E5a
   + QZSS L1/L2/L5
- All constellations and multiple frequencies RTK engine, and advanced RTK processing technology
- Independent tracking of different frequencies, and 60 dB narrowband anti-jamming

## 1.2 Key Specifications

Table 1-1 Technical Specifications

Basic Information					
Channels	1408 channels, based on NebulasIV <sup>TM</sup>				
Constellations	GPS/BDS,	/GLONASS	/Galileo/QZSS		
	GPS: L1C/	/A, L2P(W),	L2C, L5		
	BDS: B1I,	B2I, B3I			
Frequency	GLONASS	: G1, G2			
	Galileo: E1	I , E5b, E5a			
	QZSS: L1,	L2, L5			
Power					
Voltage	+3.0 V to +3.6 V DC				
Power Consumption	415 mW(Typical)				
Performance					
	Single Point		Horizontal: 1.5	5 m	
	Positionin	ıg (RMS)	Vertical: 2.5 m		
Positioning Accuracy	DGPS (RM	16)	Horizontal: 0.4 m		
Fositioning Accuracy	DGF3 (NIV	13)	Vertical: 0.8 m		
	DTV (DMC	.)	Horizontal: 0.8 cm + 1 ppm		
	RTK (RMS)		Vertical: 1.5 cm + 1 ppm		
	DDC	GPS	GLONASS	Galileo	
Observation Accuracy (RMS)	BDS	01 0			
Observation Accuracy (RMS) B1I/ L1C/A /G1/E1 Pseudorange	10 cm	10 cm	10 cm	10 cm	

B2I/L2P/G2/E5b Pseudorange	10 cm	10 cm	10 cm	10 cm
B2I/L2P/G2/E5b Carrier Phase	1 mm	1 mm	1 mm	1 mm
Time Pulse Accuracy (RMS)	20 ns		1 111111	
Velocity Accuracy (RMS)	0.03 m/s			
Time to First Fix (TTFF)	Cold Sta	rt < 30 s		
Initialization Time	< 5 s (Ty	pical)		
Initialization Reliability	> 99.9%			
Data Update Rate	5 Hz Pos	itioning		
Differential Data	RTCM 3.	0, 3.2, 3.3		
Data Format	NMEA-0	183; Unicore	!	
Physical Specifications				
Package	24 pin L0	SA.		
Dimensions	16.0 mm	× 12.2 mm	× 2.4 mm	
Environmental Specifications				
Operating Temperature	-40 °C to	+85 °C		
Storage Temperature	-55 °C to	+95 °C		
Humidity	95% No o	condensation	า	
Vibration	GJB150.	16A-2009; M	1IL-STD-810F	
Shock	GJB150.	18A-2009; M	1IL-STD-810F	
Functional Ports				
UART x 3				
I <sup>2</sup> C* x 1				

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<sup>\*</sup> Reserved interface, not supported currently.



## 1.3 Block Diagram

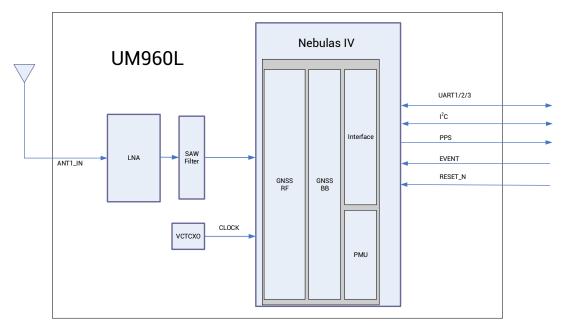


Figure 1-2 UM960L Block Diagram

#### RF Part

The receiver gets filtered and enhanced GNSS signal from the antenna via a coaxial cable. The RF part converts the RF input signals into the IF signals, and converts IF analog signals into digital signals required for NebulasIV<sup>TM</sup> chip.

### NebulasIV<sup>TM</sup> SoC

NebulasIV<sup>TM</sup> is UNICORECOMM's new generation high precision GNSS SoC with 22 nm low power design, supporting all constellations, multiple frequencies and 1408 super channels. It integrates a dual-core CPU, a high speed floating point processor and an RTK co-processor, which can fulfill the high precision baseband processing and RTK positioning independently.

#### External Interfaces

The external interfaces of UM960L include UART, I<sup>2</sup>C\*, PPS, EVENT, RESET\_N, etc.

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<sup>\*</sup> Reserved interface, not supported currently.

# 2 Hardware

## 2.1 Pin Definition

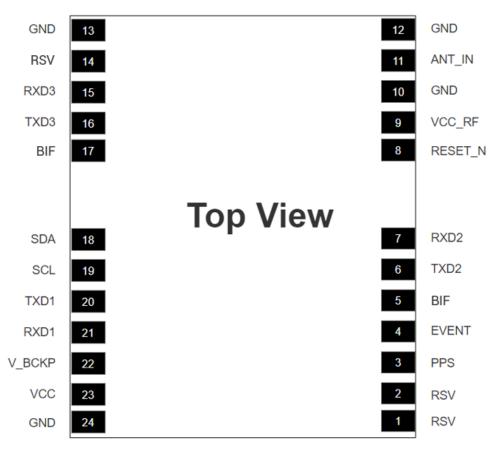


Figure 2-1 UM960L Pin Definition

Table 2-1 Pin Definition

No.	Pin	I/O	Description
1	RSV	_	Reserved, must be floating; cannot connect
ı	nov	_	ground or power supply or peripheral I/O
2	RSV		Reserved, must be floating; cannot connect
۷	Z KSV		ground or power supply or peripheral I/O
2	PPS	n	Pulse per second, with adjustable pulse width
3	PP3	U	and polarity
4	T\/FNT		Event Mark, with adjustable frequency and
4	4 EVENT		polarity



No.	Pin	I/O	Description
			Built-in function; recommended to add a
5	BIF	_	through-hole testing point and a 10 $k\Omega$ pull-up
3	טוו		resistor; cannot connect ground or power
			supply or peripheral I/O, but can be floating.
6	TXD2	0	UART2 output
7	RXD2	I	UART2 input
8	RESET_N	ı	System reset; active Low. The active time should
· · · · · · · · · · · · · · · · · · ·	NESET_IN	ı	be no less than 5 ms.
9	VCC_RF <sup>1</sup>	0	External LNA power supply
10	GND	_	Ground
11	ANT_IN	I	GNSS antenna signal input
12	GND	_	Ground
13	GND	_	Ground
1.4	DCV		Reserved; cannot connect ground or power
14	RSV	_	supply or an output interface
15	RXD3	I	UART3 input
16	TXD3	0	UART3 output
			Built-in function; recommended to add a
17	BIF	_	through-hole testing point and a 10 $k\Omega$ pull-up
17	DIF	_	resistor; cannot connect ground or power
			supply or peripheral I/O, but can be floating.
18	SDA	I/O	I <sup>2</sup> C data
19	SCL	I/O	I <sup>2</sup> C clock
20	TXD1	0	UART1 output
21	RXD1	I	UART1 input

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<sup>&</sup>lt;sup>1</sup> Not recommended to take VCC\_RF as ANT\_BIAS to feed the antenna. See section 3.2 for more details.

No.	Pin	I/O	Description
22	V_BCKP <sup>2</sup>	I	When the main power supply VCC is cut off, V_BCKP supplies power to RTC and relevant register. Level requirement: 2.0 V $\sim$ 3.6 V, and the working current is less than 60 $\mu$ A at 25 °C. If you do not use the hot start function, connect V_BCKP to VCC. Do NOT connect it to ground or leave it floating.
23	VCC	I	Supply voltage
24	GND	_	Ground

# 2.2 Electrical Specifications

# 2.2.1 Absolute Maximum Ratings

Table 2-2 Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	
Power Supply (VCC)	VCC	-0.3	3.6	V	
Voltage Input	V <sub>in</sub>	-0.3	3.6	V	
GNSS Antenna Signal Input	ANT_IN	-0.3	6	V	
RF Input Power of Antenna	ANT_IN input		+10	dBm	
mi input rower of Affterina	power		110	<u>ubili</u>	
External LNA Power Supply	VCC_RF	-0.3	3.6	V	
VCC_RF Output Current	ICC_RF		100	mA	
Storage Temperature	$T_{stg}$	-55	95	°C	

<sup>&</sup>lt;sup>2</sup> Not supported currently



## 2.2.2 Operating Conditions

Table 2-3 Operational Conditions

Parameter	Symbol	Min.	Тур.	Max.	Unit	Condition
Power Supply (VCC)	VCC	3.0	3.3	3.6	V	
Maximum Ripple Voltage	$V_{rpp}$	0		50	mV	
Working Current <sup>3</sup>	l <sub>opr</sub>		126	218	mA	VCC = 3.3 V
VCC_RF Output Voltage	VCC_RF		VCC-0.1		V	
VCC_RF Output Current	ICC_RF			50	mA	
Operating Temperature	T <sub>opr</sub>	-40		85	°C	
Power Consumption	Р		415		mW	

### 2.2.3 IO Threshold

Table 2-4 IO Threshold

Parameter	Symbol	Min.	Тур.	Max.	Unit	Condition
Low Level Input	V.	0		VCC × 0.2	V	
Voltage	$V_{in\_low}$	U		VCC × 0.2	V	
High Level Input	V	VCC × 0.7		VCC + 0.2	V	
Voltage	$V_{\text{in\_high}}$	VCC × 0.7	VGC + 0.2		V	
Low Level Output	V .	0		0.45	V	I <sub>out</sub> = 4 mA
Voltage	$V_{out\_low}$	U		0.45	V	Tout- 4 IIIA
High Level Output	V	VCC - 0.45		VCC	V	I <sub>out</sub> =4 mA
Voltage	V <sub>out_high</sub>	VCC - 0.45	VCC		V	Iout -4 IIIA

### 2.2.4 Antenna Feature

Table 2-5 Antenna Feature

Parameter	Symbol	Min.	Тур.	Max.	Unit	Condition
Optimum Input Gain	G <sub>ant</sub>	18	30	36	dB	

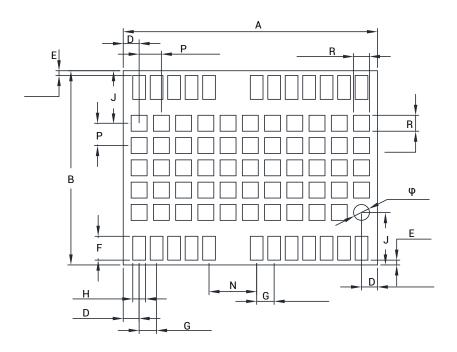
<sup>&</sup>lt;sup>3</sup> Since the product has capacitors inside, inrush current occurs during power-on. You should evaluate in the actual environment in order to check the effect of the supply voltage drop caused by inrush current in the system.

## 2.3 Dimensions

Table 2-6 Dimensions

Symbol	Min. (mm)	Typ. (mm)	Max. (mm)
A	15.80	16.00	16.50
В	12.00	12.20	12.70
С	2.20	2.40	2.60
D	0.90	1.00	1.10
E	0.20	0.30	0.40
F	1.40	1.50	1.60
G	1.00	1.10	1.20
Н	0.70	0.80	0.90
J	3.20	3.30	3.40
N	2.90	3.00	3.10
Р	1.30	1.40	1.50
R	0.99	1.00	1.10
Х	0.72	0.82	0.92
ф	0.99	1.00	1.10





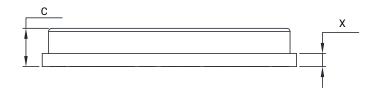


Figure 2-2 UM960L Mechanical Dimensions

# 3 Hardware Design

## 3.1 Recommended Minimal Design

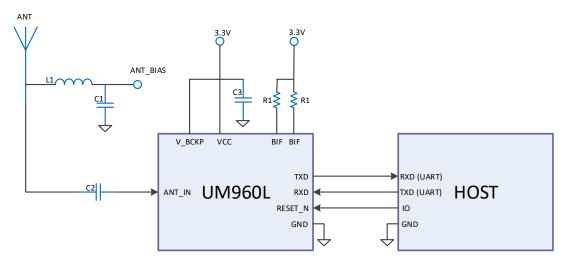


Figure 3-1 UM960L Minimal Design

#### Remarks:

- L1: 68 nH RF inductor in 0603 package is recommended
- C1: 100 nF + 100 pF capacitors connected in parallel is recommended
- C2: 100 pF capacitor is recommended
- C3:  $n \times 10 \mu F + 1 \times 100 nF$  capacitors connected in parallel is recommended, and the total inductance should be no less than 30  $\mu F$
- R1: 10 kΩ resistor is recommended



### 3.2 Antenna Feed Design

UM960L just supports feeding the antennal from the outside of the module rather than the inside. It is recommended to use devices with high power and that can withstand high voltage. Gas discharge tube, varistor, TVS tube and other high-power protective devices may also be used in the power supply circuit to further protect the module from lightning strike and surge.

If the antenna feed supply ANT\_BIAS and the module's main supply VCC use the same power rail, the ESD, surge and overvoltage from the antenna will have an effect on VCC, which may cause damage to the module. Therefore, it is recommended to design an independent power rail for the ANT\_BIAS to reduce the possibility of module damage.

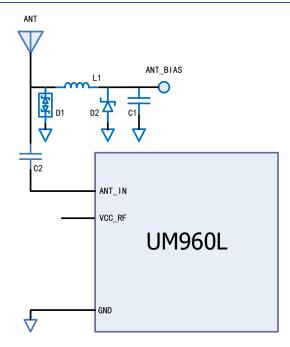


Figure 3-2 UM960L External Antenna Feed Reference Circuit

#### Remarks:

- L1: feed inductor, 68nH RF inductor in 0603 package is recommended.
- C1: decoupling capacitor, it is recommended to connect two capacitors of 100nF/100pF in parallel.
- C2: DC blocking capacitor, recommended 100pF capacitor.
- Not recommended to take VCC\_RF as ANT\_BIAS to feed the antenna (VCC\_RF is not
  optimized for the anti-lightning strike and anti-surge due to the compact size of the
  module).
- D1: ESD diode, choose the ESD protection device that supports high frequency signals (above 2000 MHz).

 D2: TVS diode, choose the TVS diode with appropriate clamping specification according to the requirement of feed voltage and antenna voltage.

### 3.3 Power-on and Power-off

#### VCC

- The VCC initial level when power-on should be less than 0.4 V.
- The VCC ramp when power-on should be monotonic, without plateaus.
- The voltages of undershoot and ringing should be within 5% VCC.
- VCC power-on waveform: The time interval from 10% rising to 90% must be within 100 µs to 1 ms.
- Power-on time interval: The time interval between the power-off (VCC < 0.4 V) to the next power-on must be larger than 500 ms.

#### **V\_BCKP**

- The V\_BCKP initial level when power-on should be less than 0.4 V.
- The V\_BCKP ramp when power-on should be monotonic, without plateaus.
- The voltages of undershoot and ringing should be within 5% V\_BCKP.
- V\_BCKP power-on waveform: The time interval from 10% rising to 90% must be within 100 µs to 1 ms.
- Power-on time interval: The time interval between the power-off (V\_BCKP < 0.4 V) to the next power-on must be larger than 500 ms.

### 3.4 Grounding and Heat Dissipation

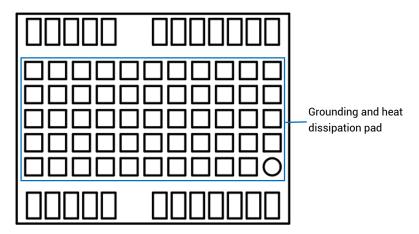


Figure 3-3 Grounding and Heat Dissipation Pad

The 55 pads in the rectangle in Figure 3-3 are for grounding and heat dissipation.

In the PCB design, they must be connected to a large sized ground to strengthen the heat dissipation.



### 3.5 Recommended PCB Package Design

See the following figure for the recommended PCB package design of the module UM960L.

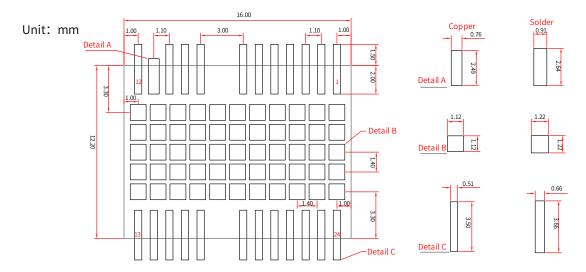


Figure 3-4 Recommended PCB Package Design

#### Remark:

- For the convenience of testing, the soldering pads of the pins are designed long, exceeding the module border much more. For example:
  - ✓ The pads denoted as detail C are 1.50 mm longer than the module border.
  - ✓ The pad denoted as detail A is 0.49 mm longer than the module border. It is
    relatively short as it is an RF pin pad, so we hope the trace on the surface is as
    short as possible to reduce the impact of interference.
- In order to effectively reduce the possibility of solder bridge during the soldering, the pin pads are designed narrower than the pins. However, the pad denoted as detail A has the same width as the pin, as we hope the resistance is as continuous as possible at the RF pin.

14 Hardware Design UC-00-M48 EN R1.1

# **4 Production Requirement**

Recommended soldering temperature curve is as follows:

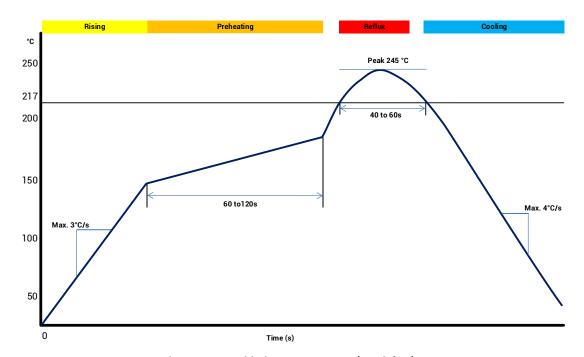


Figure 4-1 Soldering Temperature (Lead-free)

### **Temperature Rising Stage**

Rising slope: Max. 3 °C/s

• Rising temperature range: 50 °C to 150 °C

### **Preheating Stage**

• Preheating time: 60 s to 120 s

Preheating temperature range: 150 °C to 180 °C

### **Reflux Stage**

• Over melting temperature (217 °C) time: 40 s to 60 s

• Peak temperature for soldering: no higher than 245 °C

### **Cooling Stage**

Cooling slope: Max. 4 °C/s





- In order to prevent falling off during soldering of the module, do not solder it on the back of the board during design, that is, better not go through soldering cycle twice.
- The setting of soldering temperature depends on many factors of the factory, such as board type, solder paste type, solder paste thickness, etc. Please also refer to the relevant IPC standards and indicators of solder paste.
- Since the lead soldering temperature is relatively low, if using this method, please give priority to other components on the board.
- The opening of the stencil needs to meet your design requirement and comply with the examine standards. The thickness of the stencil is recommended to be 0.15 mm.

# 5 Packaging

### 5.1 Label Description



Figure 5-1 Label Description

### 5.2 Product Packaging

The UM960L module uses carrier tape and reel (suitable for mainstream surface mount devices), packaged in vacuum-sealed aluminum foil antistatic bags, with a desiccant inside to prevent moisture. When using reflow soldering process to solder modules, please strictly comply with IPC standard to conduct temperature and humidity control. As packaging materials such as the carrier tape can only withstand the temperature of 55 °C, modules shall be removed from the package during baking.



Figure 5-2 UM960L Package



Table 5-1 Package Description

Item	Description
Module Number	500 pieces/reel
Reel Size	Tray: 13"
	External diameter: 330 mm
	Internal diameter: 100 mm
	Width: 24 mm
	Thickness: 2.0 mm
Carrier Tape	Space between (center-to-center distance): 20 mm

The UM960L is rated at MSL level 3. Refer to the relevant IPC/JEDEC J-STD-033 standards for the package and operation requirements. You may access to the website <a href="https://www.jedec.org">www.jedec.org</a> to get more information.

The shelf life of the UM960L module packaged in vacuum-sealed aluminum foil antistatic bags is one year.

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